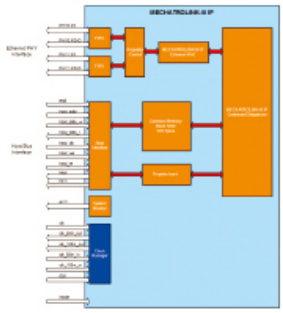
Tokyo Electron Device Ltd.

MECHATROLINK-III Master / Slave IP core

Features



MECHATROLINK-III is a communication standard meets the demands of the motion field network market that required higher transmission speed, transmission cycle, transmission distance, maximum slave number, more than ever.
By adopting this IP core provided by Tokyo Electron Device Co., Ltd. for Xilinx's FPGA enables to reduce number of parts, development cost and development period greatly.

- Master function or Slave function
- Built-in CPU in FPGA enables to perform intelligent function using RTOS with one chip
- Synchronized to a clock of up to 66 MHz, connectable to a high-speed synchronous bus such as PCI without reduced throughput

Specification

Item	Specifications
Target FPGA	Xilinx Spartan®-6 LX FPGA / Spartan-6 LXT FPGA / Zynq®-7000 SoC
Network Interface	MECHATROLINK-III Network ×2 port (MII I/F 100Mbps Full Duplex designated)
Host Interface	32bit shared memory interface / 32bit register interface
Host Interrupt	2 level Interrupt request output
Host Interface Byte Order	Little endian
Product Type	TIP-ML3MST-S6/7Z-PROJ (MECHATROLINK-III Master Dedicated IP) TIP-ML3SLV-S6/7Z-PROJ (MECHATROLINK-III Slave Dedicated IP)

Attention

To purchase this LSI, it is necessary to join the MECHATROLINK Members Association (MMA) with Board, Executive, Regular Membership.

Contact Information

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